IN THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (currently amended) A digital system comprising:

at least a first processor having an address space;

a local memory connected to the first processor and occupying a portion of the address space of the processor, the local memory operable to respond to transfer requests from the first processor, the local memory comprising a data array arranged as a plurality of segments and a plurality of indicator bits, wherein each of the plurality of segments has a corresponding indicator bit within the plurality of indicator bits; and

direct memory access (DMA) circuitry connected to the local memory, the DMA circuitry operable to transfer data to a selectable portion of segments of the plurality of segments from a selectable region of a second memory and operable to manipulate a selected portion of indicator bits of the plurality of indicator bits corresponding to the selectable portion of segments.

2. (original) The digital system of Claim 1, wherein the plurality of indicator bits are valid bits operable to indicate that a corresponding segment contains valid data; and

wherein the DMA circuitry is operable to set to a valid state the selected portion of indicator bits corresponding to the selectable portion of segments.

3. (original) The digital system of Claim 2, further comprising miss detection circuitry connected to the plurality of valid bits, the miss detection circuitry having a miss signal for indicating when a miss is detected in response to a request from the first processor to a first segment; and

wherein the processor stalls in response to the miss signal until the DMA circuitry sets a first valid bit corresponding to the first segment to a valid state.

4. (original) The digital system of Claim 3, further comprising timeout circuitry connected in a responsive manner to the miss signal having an output connected to an interrupt

input of the first processor, whereby the timeout circuit is operable to interrupt the processor if the DMA circuitry does not validate the first segment within a certain period of time.

5. (original) The digital system of Claim 2, further comprising:

miss detection circuitry connected to the plurality of valid bits, the miss detection circuitry having a miss signal for indicating when a miss is detected in response to a request from the first processor to a first segment; and

address circuitry responsively connected to the miss signal, the address circuitry operable to transfer data to the first segment in response to the miss signal.

6. (original) The digital system of Claim 5, wherein the DMA circuitry is operable to transfer a block of data to the selected portion of segments in such a manner that a transfer to the first segment holding valid data within the selected portion of segments is inhibited.

7. (original) The digital system of Claim 1, wherein the plurality of indicator bits are dirty bits operable to indicate that a corresponding segment contains dirty data.

8. (original) The digital system of Claim 7, wherein the DMA circuitry is operable to transfer data from a selectable portion of segments to a selectable region of the second memory in accordance with a corresponding portion of dirty bits, such that only segments within the selectable portion of segments whose corresponding dirty bit is in a dirty state are transferred.

9. (original) The digital system of Claim 8, wherein a first dirty bit is operable to be set to a dirty state in response to a write transaction by the first processor to a first segment associated with the first dirty bit, and

wherein the first dirty bit is operable to be set to a dirty state in response to a write transaction by the DMA circuitry to the first segment associated with the first dirty bit.

10. (original) The digital system of Claim 9, further comprising a first mode circuit connected to DMA circuitry, wherein the DMA circuitry is operable to transfer a block of segments from the local memory to the second memory in a manner that only segments within

the block marked as dirty are transferred when the first mode circuit is in a first state, and wherein the DMA circuitry is operable ignore the plurality of dirty bits such that the entire block is transferred when the first mode circuit is in a second state.

11. (original) The digital system according to Claim 1 being a cellular telephone, further comprising:

an integrated keyboard connected to the CPU via a keyboard adapter;

a display, connected to the CPU via a display adapter;

radio frequency (RF) circuitry connected to the CPU; and

an aerial connected to the RF circuitry.

12. (currently amended) A method of operating a digital system having a processor and a local memory that occupies a portion of the address space of the processor, comprising the steps of:

organizing the local memory as a plurality of segments;

associating a plurality of indicator bits with the plurality of segments such that each segment has at least one corresponding indicator bit; and

setting a first indicator bit associated with a first segment in the local memory to a first state in response to a direct memory access (DMA) transfer of a first data value from a selectable location in a second memory to the first ~~location~~ segment in the local memory.

13. (new) The method of Claim 12, wherein the plurality of indicator bits are valid bits operable to indicate that a corresponding segment contains valid data; and

wherein the step of setting comprises setting to a valid state a selected portion of indicator bits corresponding to a selected portion of segments.

14. (new) The method of Claim 13, further comprising the steps of:

detecting a miss when a requested segment is indicated as invalid in response to a request from the first processor to a first segment; and

stalling the processor in response to the detected miss until the DMA transfer sets a first valid bit corresponding to the first segment to a valid state.

15. (new) The method of Claim 14, further comprising the step of interrupting the processor if the DMA transfer does not validate the first segment within a certain period of time.

16. (new) The method of Claim 14, wherein the step of stalling stalls the processor until a block of data is transferred to the selected portion of segments.

17. (new) The method of Claim 12, wherein the plurality of indicator bits are dirty bits operable to indicate that a corresponding segment contains dirty data.

18. (new) The method of Claim 17, further comprising the step of transferring data from a selected portion of segments to a selected region of the second memory in accordance with a corresponding portion of dirty bits, such that only segments within the selected portion of segments whose corresponding dirty bit is in a dirty state are transferred.

19. (new) The method of Claim 18, further comprising the steps of

setting a first dirty bit to a dirty state in response to a write transaction by the first processor to a first segment associated with the first dirty bit, or

setting the first dirty bit to a dirty state in response to a DMA write transaction to the first segment associated with the first dirty bit.

20. (new) The method of Claim 17, further comprising the steps of:

setting a fill mode to a selected state; and

transferring a block of segments from the local memory to the second memory in a manner that either only segments within the block marked as dirty are transferred when the fill mode is in a first state, or all segments of the block of segments are transferred regardless of the associated dirty bits when the fill mode is in a second state.